



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/976,004	10/15/2001	Amit S. Phadnis	CSCO-010/4390	9588

26392 7590 06/12/2006
LAW FIRM OF NAREN THAPPETA
C/O LANDON IP, INC.
1700 DIAGONAL ROAD, SUITE 450
ALEXANDRIA, VA 22314

EXAMINER

WILSON, ROBERT W

ART UNIT	PAPER NUMBER
----------	--------------

2616

DATE MAILED: 06/12/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/976,004

Applicant(s)

PHADNIS ET AL.

Examiner

Robert W. Wilson

Art Unit

2616

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 19 May 2006.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-4, 7-16, 21-38, 43, 44, 53, 58-61, 65-72 and 76-78 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 16, 21-23, 38, 43, 44, 53 and 58 is/are allowed.
- 6) ☒ Claim(s) 1, 7-14, 24-26, 30-37, 53, 58, 59, 65-70, 72 and 76-78 is/are rejected.
- 7) ☒ Claim(s) 2-3, 15, 27-29, 60-61, & 71 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

Withdrawn Finality

1. The indicated allowability of claims 1-4, 7-16, 21-38, 43-44, 53, 58-61, 65-72, and 76-78 are withdrawn in view of the newly discovered reference(s) to Spiegel (U.S. Patent: 5,649,108) and Bare (U.S. Patent No.; 6,151,635) . Rejections based on the newly cited reference(s) follow.

Allowable Subject Matter

2. Claims 16, 21-23, 38, 43, 44, 53, & 58 are allowed.

The following is an Examiner's statement of reasons for allowance:

The closest prior art is Spiegel (U.S. Patent No.; 5,649,108) and Bare (U.S. Patent No.: 6,151,635). Spiegel teaches: a node or first end system which sends message or first signaling request per Fig 3 through the network of Fig 1 to a second node or second end system. The second node or second end system returns the message of Figure 3 with Record Route and Cumulative cost which the examiner has interpreted as an acceptance message. Once all of the path data comes back the node determines which is the least cost path and provisions that path to the second node while storing more costly routes in a routing table or not-as-yet provisioned virtual circuits. Bare teaches: that when a primary connection fails and a router switches to a backup route in order to maintain a connection to the second node.

Claims 16, 21-23, 38, 43, 44, 53, & 58 are considered allowable since when reading the claims in light of the specification, none of the references of record alone or in combination disclose or suggest the combination of limitations specified in the independent claims including:

“completing provisioning of said at least one of said not-yet provisioned virtual circuits; and sending a completion message indicating said at least one of said not-yet-provisioned virtual circuits have been activated” as specified in claim 16.

“wherein said inbound interface receives a second signaling message requesting activation of at least one of said not-yet-provisioned virtual circuits comprised in said plurality of virtual circuits, and wherein said call control logic completes provisioning of said at least one of said not-yet-provisioned virtual circuits and then sends a completion message indicating said at least one of said not-yet-provisioned virtual circuits have been activated” as specified in claim 38.

“means for completing provisioning of said at least one of said not-yet-provisioned virtual circuits and means for sending a completion message indicating said at least one of said not-yet-provisioned virtual circuits have been activated as specified in claim 53.

Claim Objections

3. Claims 2-4, 15, 27-29, 60-61, & 71 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 24-25, 30, & 32-37 are rejected under 35 U.S.C. 102(e) as being anticipated by Spiegel (U.S. Patent No.: 5,649, 108)

Art Unit: 2616

Referring to claim 24, Spiegel teaches: Figure 2 shows a device which is present in each node of Fig 1. The device is for setting up virtual circuits between a first node or first end system and a second node or second end system. The plurality of virtual circuits are set up on the network per Fig 1 connect a first node or first end system and the second node or second end system. The first node or first end system comprising: an outbound interface (10 per Fig 2) which is coupled to the network per Fig 1. The switch controller (12 per Fig 2) has inherent logic to construct the message per Fig 3. The switch controller is coupled to the outbound interface (10 per Fig 2). The switch controller has an inherent call control logic for causing the message construction block to construct a first signaling message requesting as shown in Fig 3. The message per Fig 3 requests the plurality of virtual circuits to be set up are defined to be setup per Fig 3. The first signaling message per Fig 3 is sent to the network Fig 1 to the second node per Fig 1 or second end system.

In Addition Spiegel teaches:

Regarding claim 25, Each node per Fig 1 has a host terminal per col. 4 line 64 which has an inherent external application. The host terminal sends a request for a connection to the first node or first end system per Fig 1. The first node of first end system receives the request which is processed via an inherent application program in the switch controller. The switch controller communicates internally to the inherent call control logic in order to create the first signaling message per Fig 3 which is sent in response to the request.

Regarding claim 30, 21 per Fig 2 or inbound interface receives the returned message which is in the structure of Fig 3. The message has the Record Route which is interprets as a received

Art Unit: 2616

acceptance message. The received route indicates the plurality of switches in the connection path between the first node or first end system and the second node or second end system.

Regarding claim 32, the device has a switch controller which has routing table and node memory per Fig 2 which stores the plurality of virtual circuits between the first end system and the second end system in groups which are bundled based upon cost as shown in Fig 6.

Regarding claim 33, the device has a the switch controller which has routing table and node memory per Fig 2 which store routes and associated costs or plurality of call reference structure and plurality of per-VC structure. The examiner has interpreted sending the message or Fig 3 as a call. These tables store the parameters received which tells the structure of the network corresponding to the message send or call. The route store is a VC structure which relates to the SA, DA, and Source Router or plurality of call parameters per Fig 3.

Regarding claim 34, the device has a Table stored in the Line Interface which has an IP which has an ID which maps the VC associated with the virtual circuits inbound direction to another virtual circuit outbound per Fig 2.

Regarding claim 35, the message of Fig 3 has a SA, DA, and Source Route which are a bundle identifier which are propagated without translation by each of said plurality of switches per Fig 1.

Regarding claim 36, Figure 3 defines both the first signaling message and the acceptance message format with common fields.

Art Unit: 2616

Regarding claim 37, Figure 3 SA, DA, and Source Route define the traffic parameters and Record Route defines the range.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

7. Claims 1, 7-11, 13-14, 31, 59, & 65-69 are rejected under 35 U.S.C. 103(a) as being unpatentable over Spiegel (U.S. Patent No.: 5,649,108) in view of Bare (U.S. Patent No.: 6,151,635)

Referring to claim 1, Spiegel teaches: Figure 2 shows a device which is present in each node of Fig 1. The device performs the method for setting up virtual circuits between a first node or first end system and a second node or second end system. The plurality of virtual circuits are set up on the network per Fig 1 connect a first node or first end system and the second node or second end system. The virtual circuits inherently terminate on the first node or first end system and the 2nd node or second end system. A first node per Fig 1 or first end system sends a first signaling message per Fig 3 requesting a plurality of virtual circuits (Source Route per Fig 3)

The second node or second end system per Fig 1 receives the acceptance message per Fig 3 with values in the Record Router field which the examiner has interpreted as an acceptance message.

The Record route defines the connection path between the first node or first end system and the second node or second end system between the switches and defines the virtual circuits. The routing table now has multiple routes to the second node which the examiner interprets as

Art Unit: 2616

plurality of virtual circuits. The first node or first end station immediately provisions the Least cost route per Figure 6 while storing the other routes or provision fewer than said plurality of virtual circuits.

Spiegel does not expressly call for: sending a second signaling message to activate at least one of a plurality of not-as-yet provisioned virtual comprised in said plurality of virtual circuits.

Bare teaches: When a connection of a primary network is broken the router will transfer data packet to a backup route stored in a router table per col. 1 lines 50-63 or to activate at least one of a plurality of not-as-yet provisioned virtual comprised in said plurality of virtual circuits.

It would have been obvious to add the to activate at least one of a plurality of not-as-yet provisioned virtual comprised in said plurality of virtual circuits of Bare to the method of Spiegel in order to build a system in which reconfigures around a network link failure.

In Addition Spiegel teaches:

Regarding claim 7, the routing table and node stores a plurality routes associated virtual circuits and cost per Fig 2 and Fig 6. Only the least cost route is selected or provisioning only one virtual circuit in response to the signaling message per Fig 3.

Regarding claim 8, the device has a switch controller which has routing table and node memory per Fig 2 which stores the plurality of virtual circuits between the first end system and the second end system in groups which are bundled based upon cost as shown in Fig 6.

Regarding claim 9, the device has a the switch controller which has routing table and node memory per Fig 2 which store routes and associated costs or plurality of call reference structure

Art Unit: 2616

and plurality of per-VC structure. The examiner has interpreted sending the message of Fig 3 as a call. These tables store the parameters received that tells the structure of the network corresponding to the message send or call. The route store has a VC structure that relates to the SA, DA, and Source Router or plurality of call parameters per Fig 3.

Regarding claim 10, the device has a Table stored in the Line Interface which has an ID which maps the VC associated with the virtual circuits inbound direction to another virtual circuit outbound per Fig 2.

Regarding claim 11, the message of Fig 3 has a SA, DA, and Source Route which are a bundle identifier which are propagated without translation by each of said plurality of switches per Fig 1.

Regarding claim 13, Figure 3 defines both the first signaling message and the acceptance message format with common fields.

Regarding claim 14, Figure 3 SA, DA, and Source Route define the traffic parameters and Record Route defines the range.

Regarding claim 31, it would have been obvious to one of ordinary skill in the art at the time of the invention of changing from a primary route via virtual circuits to a secondary route via virtual circuits is switching between virtual circuits or a switched virtual circuit.

Referring to claim 59, it would have been obvious to one of ordinary skill in the art at the time of the invention to encode a program on a computer readable in order to perform the method steps

Art Unit: 2616

cited claim 1 because a processor requires that the program be encoded on a readable medium in order to be executable and a method requires a processor to also be executable.

In Addition Siegel teaches:

Regarding claim 65, the device has a switch controller which has routing table and node memory per Fig 2 which stores the plurality of virtual circuits between the first end system and the second end system in groups which are bundled based upon cost as shown in Fig 6.

Regarding claim 66, the device has a the switch controller which has routing table and node memory per Fig 2 which store routes and associated costs or plurality of call reference structure and plurality of per-VC structure. The examiner has interpreted sending the message or Fig 3 as a call. These tables store the parameters received which tells the structure of the network corresponding to the message send or call. The route store is a VC structure which relates to the SA, DA, and Source Router or plurality of call parameters per Fig 3.

Regarding claim 67, the device has a Table stored in the Line Interface which has has an ID which maps the VC associated with the virtual circuits inbound direction to another virtual circuit outbound per Fig 2.

Regarding claim 68, the first node or first end system and second node or second end system contain the device per Fig 2 or router. The message of Fig 3 has a SA, DA, and Source Route which are a bundle identifier which are propagated without translation by each of said plurality of switches per Fig 1.

Art Unit: 2616

Regarding claim 69, Figure 3 defines both the first signaling message and the acceptance message format with common fields.

Regarding claim 70, Figure 3 SA, DA, and Source Route define the traffic parameters and Record Route defines the range.

8. Claim 26 is rejected under 35 U.S.C. 103(a) as being unpatentable over Spiegel (U.S. Patent No.: 5,649,108) in view of Duree (5,940,393)

Referring to claim 26, Spiegel teaches the device of claim 25 and the outbound interface (21 per Fig 2) which sends the first signaling message per Fig 3 as ATM per col. 5 line 36 which inherently are made up of cells.

Spiegel does not expressly call for: SAAL output block to encapsulate the message or for the block to be coupled to the outbound interface.

Duree teaches: SAAL encapsulation is used for ATM signaling message per col. 17 lines 10-17.

It would have been obvious to one of ordinary skill in the art at the time of the invention to add SAAL encapsulation of the message of Duree and to perform this encapsulation before the outbound interface Spiegel in order to build an ATM system which interoperates with the standards based legacy ATM system.

9. Claims 72, & 77 are rejected under 35 U.S.C. 103(a) as being unpatentable over Spiegel (U.S. Patent No.: 5,649,108)

Referring to claim 72, Spiegel teaches: a first node or first end system and a second node or second end system per Fig 1. Routing tables are defined in the switch controller in each node per Fig 1, Fig 2 and Fig 6 respectively. The routing tables define a plurality of virtual circuit which

Art Unit: 2616

can be set up on a network connecting the first node or first end system to the second node or second end system. The virtual circuits inherently terminate on the first node or first end system and also inherently terminate on the second node or second end system shown in Fig 1. Each of the nodes has a Switch Controller per Fig 2 which has a processor.

The second node or second end system receives the first signaling message per Fig 3 requesting a Record Route or plurality of virtual circuits to be set up. The first node or first end system receives the acceptance message which is Fig 3 with the Record Route and Cumulative Cost values or acceptance message. The first node or first end system then selects the least cumulative cost route from a plurality of routes or fewer than a plurality of virtual circuits to the second node or second end system as shown in Fig 6A, 6B, 6C, or 6D.

Spiegel does not expressly call for: computer readable medium or sequence of instructions
Spiegel teaches: a switch controller or processor per Fig 2.

It would have been obvious to one of ordinary skill in the art at the time of the invention to encode a program on a computer readable in order to perform the method steps cited above because a processor requires that the program be encoded on a readable medium in order to be executable and a method requires a processor to also be executable.

In addition Spiegel teaches:

Regarding claim 77, the first signaling message (Fig 3) contains SA, DA, & Source Route per Fig 3 or plurality of parameters related to the range of virtual circuits. The Record Route Cumulative Cost are stored in the Routing table and Node memory in response to the SA, DA, and Source Router parameters related to the range of the virtual circuits. The plurality of parameters are transmitted once in order to find out the range of virtual circuits in the message

Art Unit: 2616

per Fig 3. The returned values are used to determine the least cost route or provision the virtual circuits based upon the received parameters.

Response to Amendment

10. Applicant's arguments with respect to claims 1-4, 7-16, 21-38, 43-44, 53, 58-61, 65-72, and 76-78 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Robert W. Wilson whose telephone number is 571/272-3075. The examiner can normally be reached on M-F (8:00-4:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Doris To can be reached on 571/272-7629. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.



DORIS H. TO
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600



Robert W Wilson